FPGA AND ASIC DESIGN

1.1. Course number

18483

1.2. Course Area

Electrical Engineering.

1.3. Course type

Core Course

1.4. Course level

Undergraduate

1.5. Year

3º

1.6. Semester

1º

1.7. Número de créditos

6 ECTS credits

1.8. Prerequisites

Student must know the fundamentals of Logic Design or similar. That is, a first course on digital circuit that mainly includes Combinational Circuits, Counters, and FSM. For example: the subject Digital Electronic Circuits of the EPS UAM Program.

1.9. Minimum attendance requirement

Students must be present at least the 80% of the lessons and 100% of the Lab sessions.

1.10. Faculty data

Nota: se debe añadir @uam.es a todas las direcciones de correo electrónico.

Theory:

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1.11. Course objectives

GENERAL GOALS	
1	Lear different techniques and tools to design complex circuits
2	Design, specify or negotiate an ASIC.
3	Capability to solve problems and read technical information
4	Capacity to optimize and simplify complex circuits.
5	Capacity to learn from scientific literature papers

ESPECIFIC GOALS	
THEME 1.- INTEGRATED CIRCUITS AND SEMICUSTOM ASICS	
1.1.	Fabrication alternatives.
1.2.	Gate Arrays, Standard Cells, ASICs Estructurados.

1.3.	Transistor-level of CMOS gates.
THEME 2.- FPGA ARCHITECTURES, TECHNOLOGIES AND TOOLS	
2.1.	LUT, IOB and interconnection
2.2.	*Hard-cores*
2.3.	Steps of a professional EDA tool
2.4.	EDA algorithms
2.5.	Silicon compiler options
THEME 3.- DELAYS AND SINCHRONIZATION	
3.1	RC model. Delay and *fanout*.
3.2	Design of a clock tree. Use of digital PPLs
3.3	Single-phase sinchronization
3.4	Sinchronization faults and metaestability
3.5	Parallelism-Pipeline. Speedup, latency, and *throughput*
3.6	Tools for physical design and timing analysis
3.7	On-chip options to increase
THEME 4.- DESIGN FOR TEST (DFT)	
4.1	Ad-hoc DFT Techniques
4.2	*Stuck-at* Model
4.3	*Scan Path*, *Tesbenchs*, *ChipScope* and others tools.
4.4	DFT and Fault-tolerance
THEME 5.- ECONOMICS ASPECTS	
5.1	FPGA evolution.
5.2	Learning curve of FPGA technology.
5.3	Spanish sector on FPGA technology.

1.12. Course contents

Condensed Program

UNIT 1. **Integrated Circuitos and Semicustom ASICs**
UNIT 2. **FPGAs Architectures**
UNIT 3. **Algorithms and EDA Tools**
UNIT 4. **Delay Model**
UNIT 5. **Synchronization and Pipeline**
UNIT 6. **DFT**
UNIT 7. **Marketing of FPGAs**

Detailed Program

1. - **Integrated Circuits and Semicustom ASICs**

SSI, MSI Circuits (1960-70).
Cascadable y sliced block.
Estandarization.
Hardwired algorithms.
ASICs: Gate Array, Standard Cells, SOG, Structured FPGAs.
CMOS gates.
Masked-ASICs.

2.- FPGA Architecture

Fabless model.
LUTs, Interconections, and Configuration Memory.
LUT size and trade-offs.
Configuration. FPGA Retargeting. *Easy Path*. Antifuses.
Maximum Frequency and applications fields
Especific resources: RAM, Mult y DSP, SRL, uP, DCM, Transceivers
I/O and packaging
Xilinx vs Altera

3.- Algorithms and EDA Tools

VHDL and other languages
Design Flow
Synthesis, partitioning, place-route
Subexpresions
Shannon Cofactoring
Steimberg
Mincut and Simulated Annealing
Global and detailed routing
EDA Xilinx and options

4.- Delay Model

Capacitance. C Charge and Energy.
Tipycal values in integrated circuits. Standard Cells example.
Intrinsic delay. *Fanin* and *Fanout*.
Broadcasted signals
Clock tree, PLL and *Duty-Cycle*.
Timing analizer. Critical and false paths
Deration.
Pines, Pull-Up / Pull-Down, Bus keeper

5.- Synchronization and Pipeline

Glitches
sincronización Registros. Time parameters of a FF
Gated-clocks
Clock Skew. Metaestability.
Sinchronous design principle.
Throughput), latency, *speed-up*
Skewing y *deskewing*
Logic Depth
Coste de un pipeline.
Retiming
local and global wires.

6.- DFT

Heuristics: Observability-Controlability
Stuck-at model. Fault coverage
Scan Path and JTAG.
ChipScope.
Temperature.
DFT and Fault-tolerance
Instruments for test.

7. Marketing of FPGAs

FPGA company evolution
Learning curve
Market of FPGA and players
Invitated conferences.

1.13. Course bibliography

Bolton M., "Digital System Design with Programmable Logic", Addison-Wesley, 1990.
681.32 BOL

Brown S., Francis R. , Rose J. y Vranesic Z., "Field-Programmable Gate Arrays", Boston: Kluwer Academic Publishers, 1992.

Chan, P. and Murrad, S. "Digital Design using Field-Programmable Gate Arrays", Prentice-Hall 1994.
681.31 CHA

Francis, R. "A Tutorial on Logic Synthesis for Look-up Table Based FPGAs", ICCAD-92 Digest of Technical Papers, pp.40-47, Nov. 1992.

Jenkins J., "Designing with FPGAs and CPLDs".
681.3 JEN

Mandado, Enrique, "Dispositivos lógicos programables"
621.3 MAN

Oldfield J. and Dorf R. , "Field-Programmable Gate Arrays. Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Sistems", John Wiley & Son. 1995.
621.3 OLD

Tavernier, C. "Circutos Lógicos Programables", Editorial Paraninfo.
621.3 TAV

Trimberger S., "Field-Programmable Gate Arrays Technology", ", Boston: Kluwer Academic Publishers, 1995.
621.3 FIE

Amerasekera, E. Ajith, "Failure mechanisms in semiconductor devices".
621.315/AME

Baker J. et al., "CMOS Circuit Design, Layout, and Simulation", IEEE Press Series on Microelectronic Systems.
621.3BA

Application-Specific Integrated Circuits
Smith, Michael
INF/621.3/SM

Abramovici M. Melvin A. Breuer, Arthur D. Friedman, "Digital systems testing and testable design", 1990.
681.32/ABR

Sousa, José T. de, "Boundary-scan interconnect diagnosis"
621.38/SOU

Lall, Pradeep, "Influence of Temperature on Microelectronics and System Reliability"
621.3/LAL

Josep Altet y Antonio Rubio, "Thermal testing of Integrated circuits"
B1200/ALT